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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/620,544	07/21/2000	Petro Estakhri	38979-11CPA2	2400
27728	7590	03/03/2004	EXAMINER	
LAW OFFICES OF IMAM 111 N. MARKET STREET, SUITE 1010 SAN JOSE, CA 95113			BRAGDON, REGINALD GLENWOOD	
			ART UNIT	PAPER NUMBER
			2188	

DATE MAILED: 03/03/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary

Application No.

09/620,544

Applicant(s)

ESTAKHRI ET AL.

Examiner

Reginald G. Bragdon

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 2-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____. 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 21 January 2004 has been entered.

Information Disclosure Statement

2. It is noted that Applicant has submitted an IDS with the present amendment. However, the references were previously considered during the prosecution of the present application. Copies of the previously submitted and considered PTO-1449s were attached to paper no. 5 and paper no. 24.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

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4. Claims 2-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Hasbun et al. (5,586,285).

As per claims 2, 3, 7, 11, and 15, Hasbun et al. teaches, with reference to figures 1 and 2, a host CPU 52, a solid state disk controller 64 (“controller”), and a FLASH memory array 62 (“nonvolatile memory storage”) made up of a plurality of blocks, each comprised of a plurality of sectors (see figure 1; column 2, lines 39-42; and column 16, lines 62-64). Each sector of data within a block is identified by a logical sector number, or LSN. See column 5, lines 10-15. Therefore, each block is associated with a plurality of logical sector numbers, and the totality of blocks within the system of Hasbun et al. would be associated with all logical sector numbers (a “group of logical block addresses”), where the logical sector number must inherently include information on the particular block within which a particular desired sector resides. See also column 13, lines 50-54. A logical address is inherently mapped to a predetermined group of sectors.

With reference to figure 9, for a write operation received from the host to write a sector (“one or more sectors”) to the FLASH memory array, the updated sector is written (step 256) to another block (selected by an allocate free physical memory operation, step 250). No other sectors stored in the old block are moved, and the header information for the updated block is modified, as is the translation table pointing to the most recent version of the block (step 258). Therefore, Hasbun et al. teaches only writing the updated sector without moving the remaining sectors as described in column 16, line 59, to column 17, line 7.

As per claims 4, 8, and 12, it is inherent that further write commands to further sectors would result in the process described for claims 3, 7, and 11, being repeated.

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As per claims 5-6, 9-10, and 13-14, previous sector information will be moved at a later time, such as when the previous sector information is erased.

Response to Arguments

5. Applicant's arguments filed 21 January 2004 have been fully considered but they are not persuasive.

Applicant argues, on page 7 of the response, that Hasbun et al. does not teach "one or more blocks being identified by a group of logical block addresses corresponding to a predetermined group of sectors. However, the limitation of "a group of logical block addresses corresponding to a predetermined group of sectors" is still sufficiently broad that it reads on all logical addresses within the system of Hasbun et al., since all logical block addresses correspond to a predetermined group of sectors (i.e. a logical address is inherently mapped to a predetermined group of sectors)

Applicant mentions "block management" as a feature of the present invention (page 7 of the response). However, it is not clear how the present claims set forth "block management" in a manner that distinguishes the present claims from Hasbun et al.

Applicant cites sections of Hasbun et al. that teach moving or copying blocks (see the paragraph spanning pages 7 and 8 of the response). Although Hasbun et al. may teach moving or copying blocks, within the teachings of Hasbun, when writing a sector to the FLASH memory, blocks not being written are not moved or copied (which is what Applicant has claimed). See column 16, line 59, to column 17, line 7.

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With respect to Applicant's comments on page 8 concerning the limitation in the claims of "without moving or copying the data in the sectors...", it is reiterated that Hasbun et al. teaches only writing the updated sector without moving the remaining sectors as described in column 16, line 59, to column 17, line 7. And although Hasbun et al. may consider whether or not the sector fits in the particular block, Hasbun et al. still teaches the claim limitation of writing one or more sectors of data to one or more new blocks...without moving or copying the data in sectors in the one or more blocks that the host did not specify to be rewritten. The Examiner notes that the newly added limitation of "or copying" is set forth as alternative language, and the claim is anticipated if a reference teaches one of either "moving" or "copying".

Furthermore, although the sectors in Hasbun et al. may be compressed, Hasbun et al. is still rewriting sectors.

Conclusion

6. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(703) 872-9306**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(703) 746-5693**, only after approval by the Examiner.

Hand-delivered responses should be brought to Crystal Park II, 2121
Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

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7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (703) 306-2903.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

RGB
March 1, 2004

Reginald G. Bragdon
Reginald G. Bragdon
Primary Patent Examiner
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